Arria 10 SoM
System-on-Module Baseboard

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System-on-Module

The Dream Chip Arria 10 SoM Base Board is an evaluation board for the Arria 10 System-on-Module comprising DisplayPort and 12G SDI video input and output interfaces. Dream Chip provides an adapter board that expands the on board FMC-Connector to 6 BCON interfaces for sensor applications.

Additional board features include 1GBit Ethernet, 10Gbit Ethernet, PCIe Gen3 x4, USB 2.0 Host/Device, USB UART, Video Genlock input, FMC Expansion Connector and LEDs.
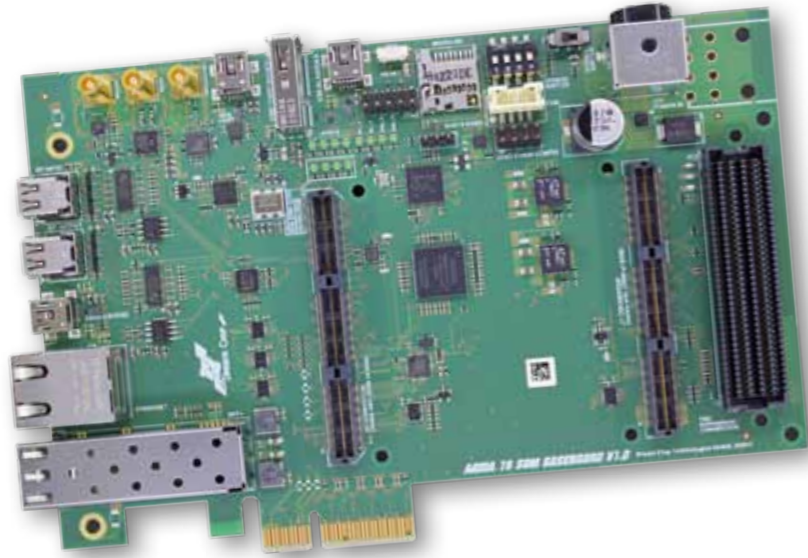
Overview

- Arria 10 SoM Base Board
- PCIe Board or stand alone operation
- High speed Video I/O
- High speed Data I/O
- Expansion port (FMC, 32x LVDS)
- Debug and control interfaces

Benefits

- Official reference design
- Custom sensor interfaces supported via FMC
- Remote system control

Base board interfaces

- PCIe Gen 3 x4
- DisplayPort 1.2 (up to 4k)
- 12G SDI up to 2160p60
- Video Genlock via trilevel sync
- Gigabit Ethernet (RJ45)
- 10Gbit Ethernet (SFP+)
- Mini-USB (Data I/O and Debug)
- USB Host port
- FMC-Connector for board expansion

Dimensions

- Short PCIe card (168 x 111mm)

Contact

Product Information

The Arria 10 SoM was developed with an emphasis on embedded and automotive vision applications. Using Intels Arria 10 SoC devices in the 29x29 mm package, the module off ers a multitude of interfaces in a small 8 cm by 6,5 cm form factor.

Using a System on Module has many advantages for customers since the most difficult challenges of using an FPGA like the Arria 10 have already been solved, such as DDR4 layout, transceiver breakout and power supply. By using two long, slim 180 pin connectors with two rows of 0.5 mm pitch pins on each side it is easy for the customer to design a cost efficient base board with just a few copper layers while using the extensive IO connectivity of the Arria 10 SoM.

The two separate memory interfaces allow the ARM Cortex-A9 subsystem and the FPGA to handle bandwidth intensive applications such as frame buffering and object detection to proceed in parallel without bandwidth bottlenecks, especially for high frame rate, 3D and 4K applications.

32 versatile LVDS lanes are brought out to the module connectors, allowing a variety of customer specific high speed differential data IO with e.g. image sensors, displays, ADC or DACs. Each lane can individually be used as 2 independent 1.8V GPIOs as well to be able to e.g. hook up single ended control & status signals or other generic IO functions. All 12 RX/TX Gigabit transceivers can be used to implement high bandwidth video standards such as 12G SDI or DisplayPort. This requires a careful clocking strategy to minimize jitter for sensitive applications such as SDI. The four transceiver reference clock pins are partly connected to programmable clock generators on the module itself, the others are sourced from the base board to implement interfaces like PCIe Gen3 where the reference clock comes from the system or to allow for video genlocking.

Full potential of the ARM Cortex A9 subsystem

The module off ers quick boot times with a dedicated QSPI Flash for the ARM subsystem, next to the bulk storage of an eMMC module of up to 16 GB for a linux file system. An optional SD card slot can be realized on the baseboard. Most of the dedicated ARM peripheral IP can be utilized, with an Ethernet PHY and one USB PHY (Device) directly on the module. A second USB (OTG) or 1G-Ethernet interface can be realized on the baseboard with an additional USB PHY chip controlled via ULPI interface.

Prepared for industrial environments

All components on the module are certified for industrial temperature grade, and the chosen connectors are ready for vibration intensive environments. To ease the integration into industrial environments, where >1.8V IO is still common, the module off ers level shifters with user provided reference I/O voltage for the ARM/HPS I2C, SPI & GPIO interface signals.

Made for vision

The high count of LVDS lanes and the high memory bandwidth make this module the right choice for demanding vision applications. Up to 8 image sensors with 6.4Gbit/s video data each can e.g. be connected for ADAS applications such as surround view for larger vehicles like busses or trucks. Due to the large amount of available logic 3D stereo vision with computing intense algorithms implemented in OpenCL is possible on just one module.

Evaluation Baseboard

Next to the module itself, Dream Chip provides a fully featured baseboard to evaluate the module and accelerate development. It comes in form of a short PCIe x4 card and includes interfaces such as DisplayPort in/out, 10 Gigabit Ethernet, 12G SDI, 2x USB, 1G Ethernet and an FMC connector that connects most of the LVDS and IO to extension cards.

System on Module Features

- 8x6,5 cm Module with two mezzanine connectors to a customer base board
- Intel Arria 10 SoC FPGA with 160 to 480 KLEs and Cortex A9 Dual Core CPU
- Power management on the module guarantees proper power-up and -down sequence, only 12V to be supplied by baseboard

- Two separate DDR4 memory interfaces
- CPU Memory System
  - 2GByte
  - 32 Bit parallel Data Bus
  - 8 Bit ECC supported for safety critical applications
  - Up to 2.4Gbit/s per pin for a total bandwidth of 77Gbit/s

- FPGA Memory System
  - 4GByte
  - 64 Bit parallel Data Bus
  - Up to 2.4Gbit/s per pin for a total bandwidth of 153Gbit/s
- All 12 Transceivers at 12 GBit/s and above:
  - Supports interfaces such as PCIe Gen3 x8, 10/40 GBit/s Ethernet, DisplayPort and 12G SDI
  - Dedicated clocking on the module to provide lowest jitter for sensitive applications such as SD
- Up to 32 LVDS lanes to the baseboard:
  - each either RX or TX
  - support for soft clock recovery
  - up to 1.6 Gbit/s per lane
  - four dedicated clock inputs/outputs that allow configurations such as two LVDS TX x8 interfaces and another two LVDS RX x8 interfaces
- Two USB interfaces, one of them OTG (ULPI interface, separate PHY required on baseboard)
- Gigabit Ethernet
- ARM I²C, SPI & GPIO interface signals with levelshifters on the module (user provides desired reference voltage of 1.8-3.3V)
- UART, 6x, 6x 1V8 GPIO from the ARM and FPGA to the baseboard
- Up to 6x I²C interfaces

Reference Designs

In order to accelerate customer development, the Intel Arria 10 Golden System Reference Design has been ported to the module. It includes the FPGA design with preconfigured IP for the HPS and memory controllers, as well as a customized Uboot and Angström Linux distribution. Dream Chip also offers software to configure the on-module programmable clock generator with the customers clocking requirements. Additional example designs will be available soon, such as 4K DisplayPort Input/output, 12 G SDI camera input and multiple camera surround view.